BU03 Specification

Version V1.1.0

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Document resume

Version	Date	Develop/revise content	Edition	Approve
V1.0.0	2024.06.11	First Edition	XiHuan Lv	Ning Guan
V1.1.0	2024.07.24	Modify antenna form, appearance diagram, pin diagram, power consumption value, schematic diagram	XiHuan Lv	Ning Guan

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1. Product Overview

BU03 is an ultra wideband (UWB) module designed by Ai-Thinker Co., Ltd. based on Decawave's DW3000 series chip. BU03 integrates onboard ceramic antenna, RF circuit, power management. BU03 can be used in bidirectional ranging, TDOA or PDOA positioning systems, positioning accuracy can reach 10 cm and data rates of up to 6.8 Mbps are supported. It can be widely used in precision positioning, coal mine positioning, hospital personnel positioning, storage positioning, various indoor positioning and other fields.

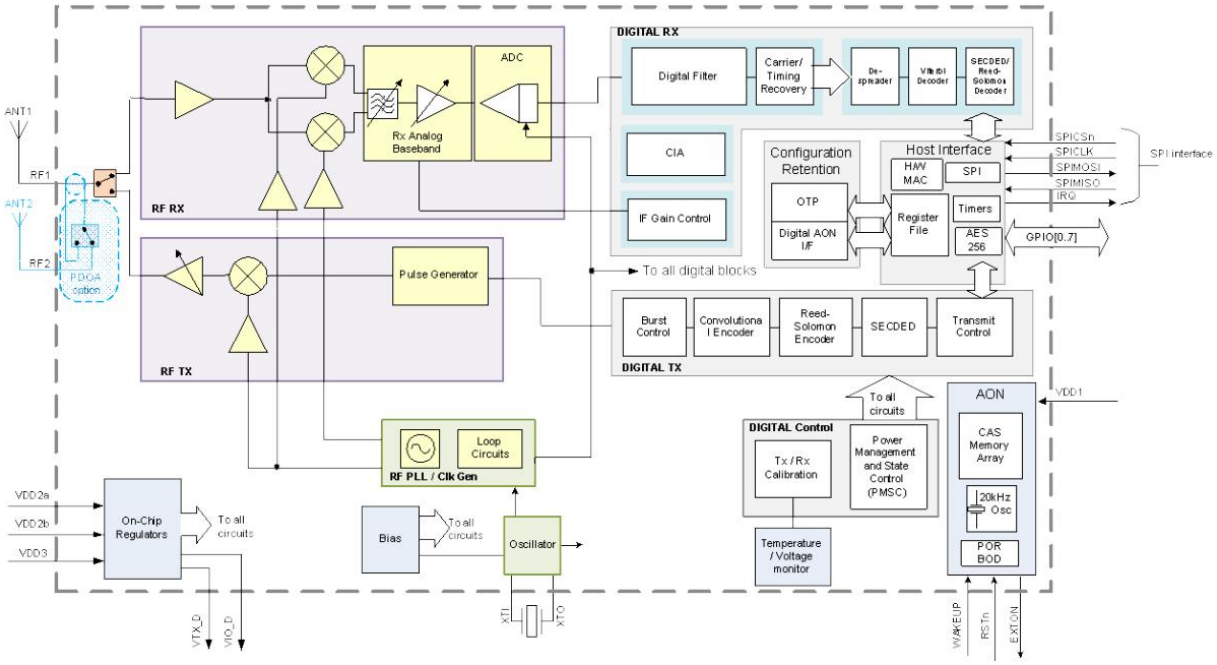


Figure 1 Main chip architecture diagram

1.1. Characteristic

- SMD-24 package
- Complies with IEEE 802.15.4-2015 UWB standard
- Complies with IEEE802.15.4z（BPRF mode）
- Supports channel 5 and channel 9
- Easy integration without RF design
- Integrated MAC support
- Extends the range of communication using the RTLS infrastructure
- Data rate 850 Kbps, 6.8 Mbps
- Supports bidirectional ranging and TDOA and PDOA positioning schemes
- Provides accurate positioning and data transmission
- Positioning accuracy 10 cm
- Supports high label density
- Integrated HW AES 256
- Support SPI interface
- 9 GPIO available
- Programmable adjustment of the transmit power
- The power supply voltage ranges from 2.5 V to 3.6 V
- Power consumption <1uA in sleep mode
- For button battery solutions

2. Main parameters

Table 1 Description of the main parameters

Model	BU03
Package	SMD-24
Size	23.0*13.0*2.5(±0.2)mm
Antenna	Onboard ceramic antenna
Center frequency	CH5(6489.5MHz),CH9(7987.2MHz)
Operating temperature	-40℃~ 85℃
Storage temperature	-40℃~ 125℃, < 90%RH
Power supply	Supply voltage 2.5V ~ 3.6V, typical value 3.3V. Power supply current ≥200mA
Interface	SPI
IO	9

2.1. Static electricity requirements

BU03 is an electrostatic sensitive device, special precautions must be taken when handling it.

Figure 2 ESD anti-static diagram

2.2. Electrical characteristics

Table 2 Electrical characteristics table

Parameter		Name	Min.	Typical value	Max.	Unit
Supply voltage		VDD	1.7	3.3	3.6	V
Supply voltage		VCC	2.5	3.3	3.6	V
I/O	VIL	-	-	-	0.3*VDD	V
	VIH	-	0.7*VDD	-	-	V
	VOL	-	-	0.1*VDD	-	V
	VOH	-	-	0.9*VDD	-	V
	IMAX	-	-	-	10	mA

2.3. RF Parameters

Table 3 UWB RF parameters

Description	Typical value	Unit
CH5 center frequency	6489.6	MHz
CH9 center frequency	7987.2	MHz
Channel bandwidth	499.2	MHz

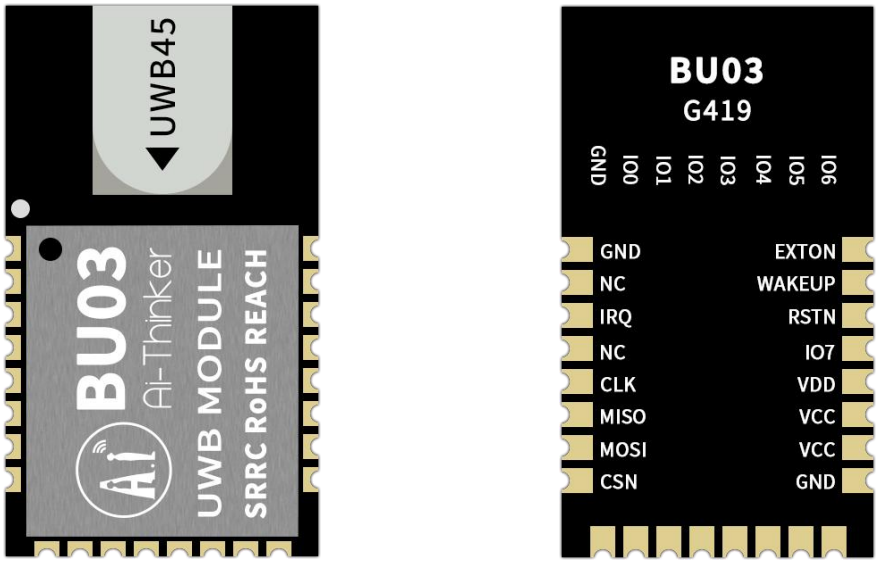
2.4. Power Consumption

The following power consumption data is based on a 3.3V power supply and an ambient temperature of 25° C.

Table 4 Power consumption table

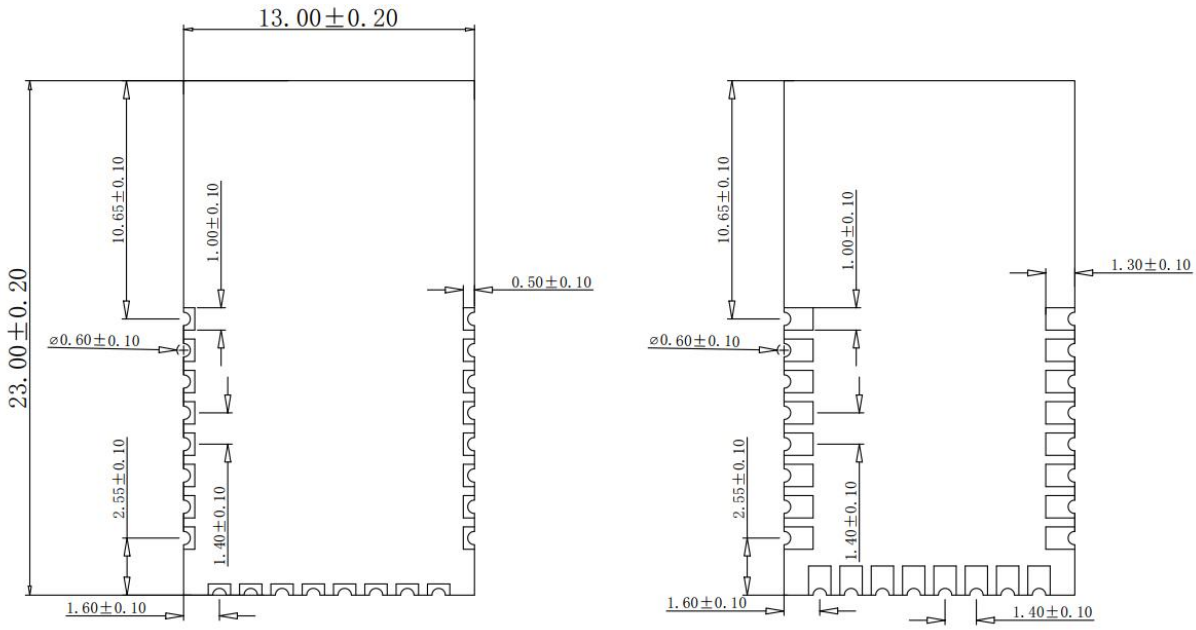
Mode	Min.	Typical value	Max.	Unit
CH5 transmitting at 0.85Mbps	-	18.77	-	mA
CH5 transmitting at 6.81Mbps	-	16.25	-	mA
CH9 transmitting at 0.85Mbps	-	26.43	-	mA
CH9 transmitting at 6.81Mbps	-	24.89	-	mA
CH5 receives at 0.85Mbps	-	44.17	-	mA
CH5 receives at 6.81Mbps	-	44.14	-	mA
CH9 receives at 0.85Mbps	-	53.97	-	mA
CH9 receives at 6.81Mbps	-	53.74	-	mA
Instantaneous start-up current	-	176	-	mA
Deep sleep	-	142	-	nA

3. Appearance dimensions



Front Back

Figure 3 Appearance of the module(the rendering is for reference only, the actual object shall prevail)



Front Back

Figure 4 Module size diagram

4. Pin definition

BU03 module has a total of 24 pins, such as the pin schematic diagram, and the pin function definition table is the interface definition.

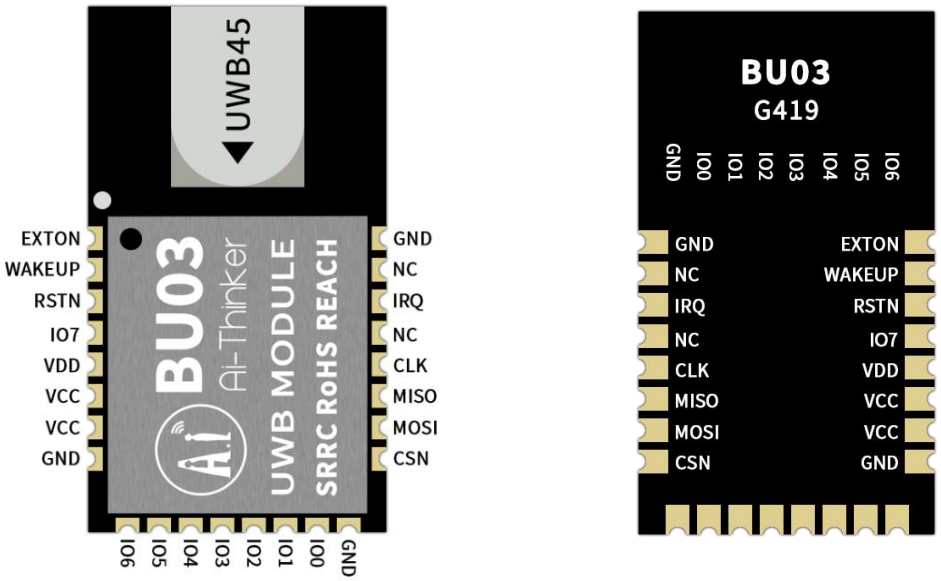


Figure 5 Schematic diagram of module pins

Table 5 Pin function definition tabled

No.	Name	Function	Power domains
1	EXTON	External devices are enabled. Takes effect during wake up and remains active until the device enters sleep mode. Can be used to control external DC-DC converters or other circuits that are not needed when the device is in sleep mode to minimize power consumption	VDD
2	WAKEUP	When activated as high state, the WAKEUP pin brings the DW3000 from sleep or DEEPSLEEP state into operational mode. If not in use, it should be grounded	VDD
3	RSTN	Chip reset pin, low active. Can be pulled down by an external leaky drive to reset the DW3000. Cannot be pulled up by an external power supply. The effective RSTn pin will reset the device completely, equivalent to a single power cycle.	VDD
4	IO7	GPIO7/SYNC, the SYNC input pin is used for external synchronization. When the SYNC input function is not used, this pin can be reconfigured as a universal I/O pin that is pulled	VDD
5	VDD	The power supply ranges from 1.8V to 3.6V. The recommended output current of the external power supply is more than 200mA	VDD

6	VCC	The power supply ranges from 2.5V to 3.6V. The recommended output current of the external power supply is more than 200mA	VCC
7	VCC	The power supply ranges from 2.5V to 3.6V. The recommended output current of the external power supply is more than 200mA	VCC
8	GND	Ground	GND
9	IO6	GPIO6/EXTRXE/SPIPHA, universal I/O pin. When powered on, it acts as a SPIPHA (SPI Phase Selector) pin to configure the SPI mode of operation. It can be configured to be used as EXTRXE (external receiver enabled). When the DW3000 is in receive mode, this pin becomes higher. When powered on, the pin will default to the universal I/O pin	VDD
10	IO5	GPIO5/EXTTXE/SPIPOL, universal I/O pin. When powered on, it acts as a SPIPOL (SPI Polarity Selection) pin to configure the SPI mode of operation. When powered on, the pin will default to the universal I/O pin. It can be configured to be used as EXTTXE (External transport enabled). When the DW3000 is in	VDD
11	IO4	GPIO4/EXTPA, universal I/O pin. It can be configured as an EXTPA (External Power Amplifier). This pin enables an external power amplifier	VDD
12	IO3	GPIO3/TXLED, universal I/O pin. It can be configured as a TXLED driver pin, which can be used to light up the LED after transmission.	VDD
13	IO2	GPIO2/TXLED, universal I/O pin. It can be configured to be used as an RXLED driver pin, which can be used to light the LED during the receive mode	VDD
14	IO1	GPIO1/SFDLED, universal I/O pin. It can be configured to be used as the SFDLED drive pin, which can be used to light the LED when the receiver finds the SFD (frame start separator)	VDD
15	IO0	GPIO0/RXOKLED, universal I/O pin. It can be configured to be used as an RXOKLED driver pin, which can be used to light up the LED when a good frame is received	VDD
16	GND	Ground	GND
17	CSN	SPICSn, SPI chip selection. The high-to-low conversion on the SPICSn signals the start of a new SPI transaction. SPICSn can also be used as a wake up signal to bring the DW3000 out of SLEEP or DEEPSLEEP.	VDD
18	MOSI	SPI data input	VDD
19	MISO	SPI data output	VDD
20	CLK	SPI clock input	VDD
21	NC	Empty pin	-

22	IRQ	GPIO8/IRQ, universal I/O pin. Interrupt request output from DW3000 to host processor. By default, IRQ is effectively high output, but can be configured to be low effective if desired. In order to operate correctly in both SLEEP and DEEPSLEEP modes, it should be configured to be active and highly effective. The pin will float in the SLEEP and DEEPSLEEP states and may cause a false interrupt on the host unless externally pulled down (100kΩ recommended). When the IRQ function is not used, the pin can be reconfigured as a general purpose I/O line	VDD
23	NC	Empty pin	-
24	GND	Ground	GND
Note: 1. All GPIO pins have a software-controlled internal pull-down resistor except for SPICSn, which has a pull-up function to ensure safe operation when the input pin is not driven. The value of the internal resistor can vary with the VDD supply voltage, ranging from 10 kΩ (1.8V for VDD) to 30 kΩ.			

5. Schematic

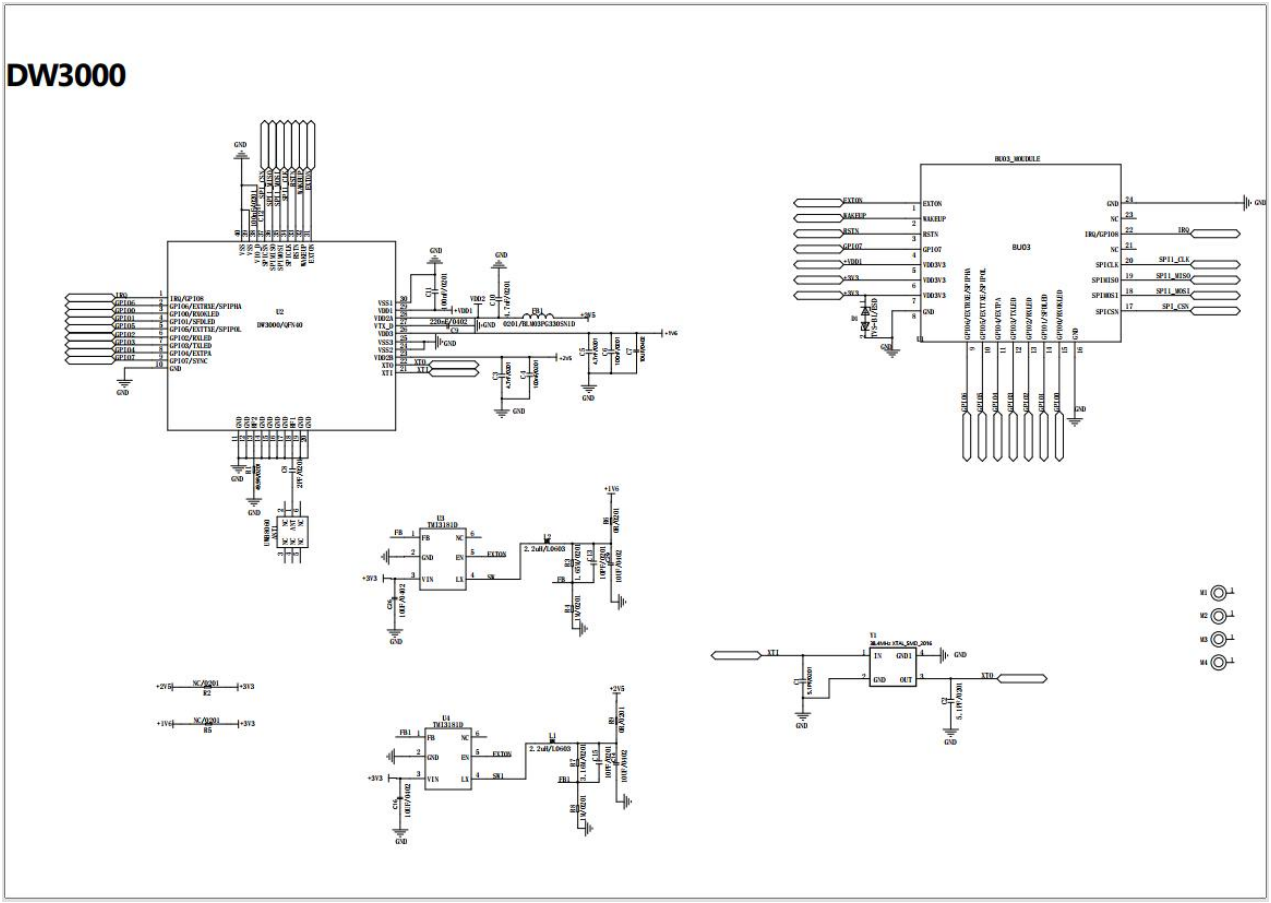


Figure 6 Module Schematic

6. Antenna parameters

6.1. Antenna test prototype

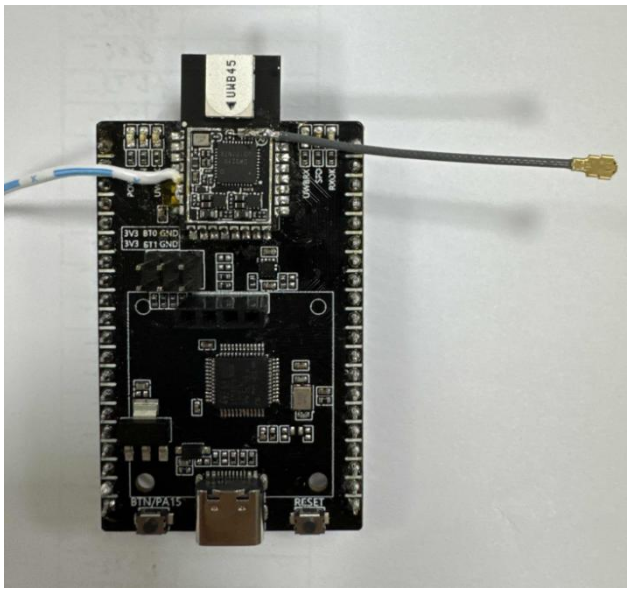


Figure 7 Schematic diagram of antenna test prototype

6.2. Antenna S parameter

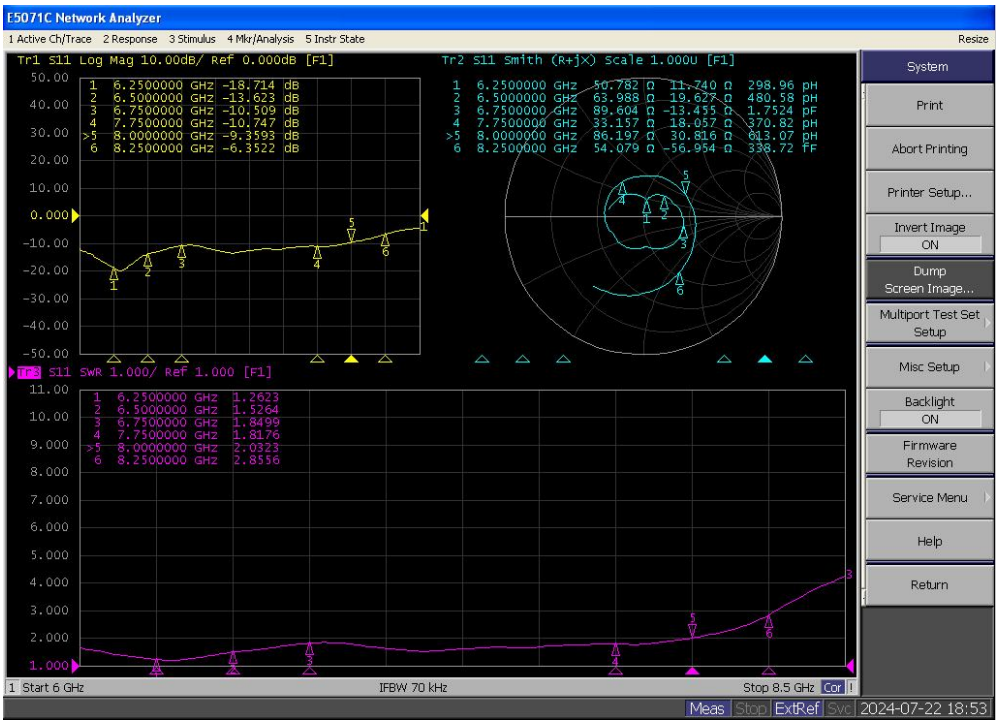


Figure 8 Antenna S parameters

6.3. Application Guidance Circuit

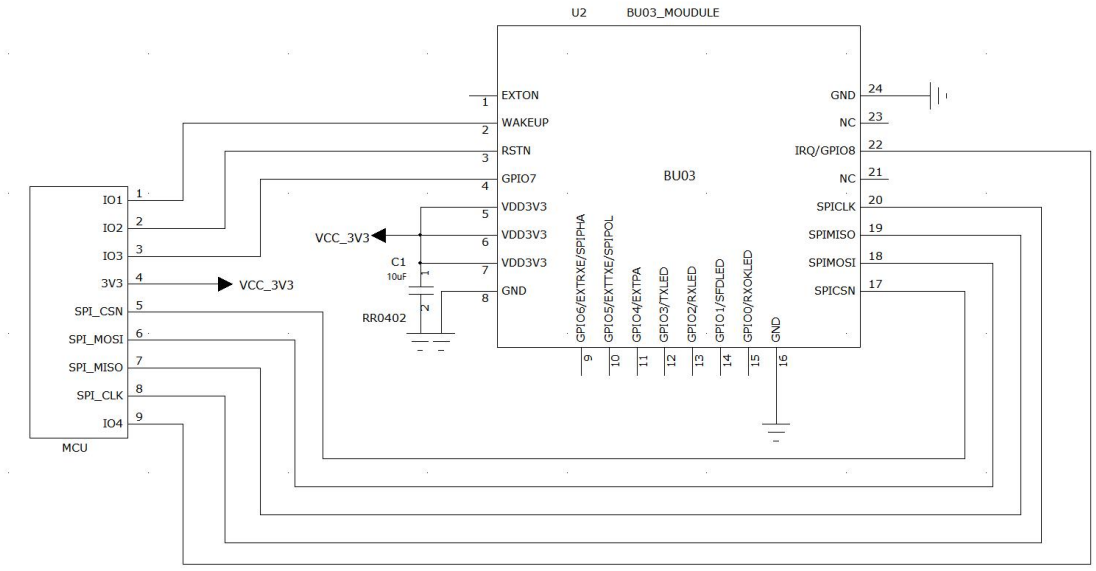


Figure 9 Application guidance circuit

6.4. Recommended PCB package size

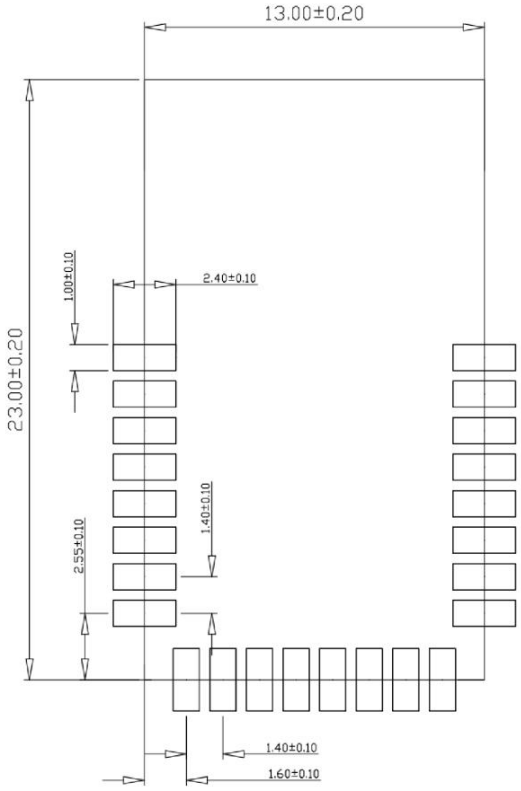


Figure 10 Recommended PCB package size

6.5. Antenna layout requirements

- Advised to use the following two methods to determine the installation position on the main-board:
  Solution 1: Put the module on the edge of the motherboard, and the antenna area extends out of the motherboard edge.
  Solution 2: Put the module on the edge of the motherboard, and the edge of the motherboard hollows out an area at the antenna position.
- To meet the performance of the onboard antenna, do not place metal parts around the antenna and keep it away from high-frequency devices.

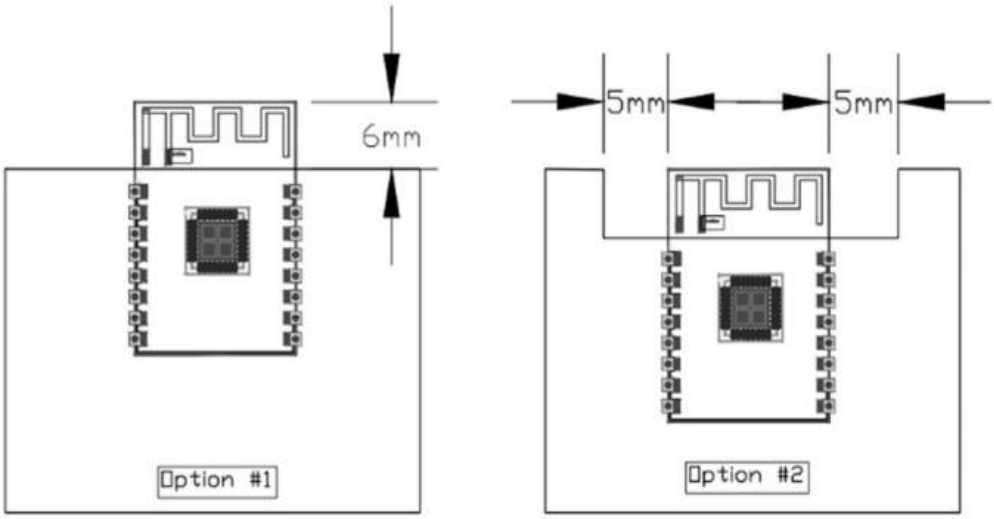


Figure 11 Schematic diagram of antenna layout

6.6. Power supply

- Recommended 3.3V voltage, peak current above 200mA.
- LDO power supply is recommended; If DC-DC is used, it is recommended to control the ripple within 30mV.
- DC-DC power supply circuit It is recommended to reserve a dynamic response capacitor to optimize output ripple when the load changes greatly.
- ESD devices are recommended for the 3.3V power port.

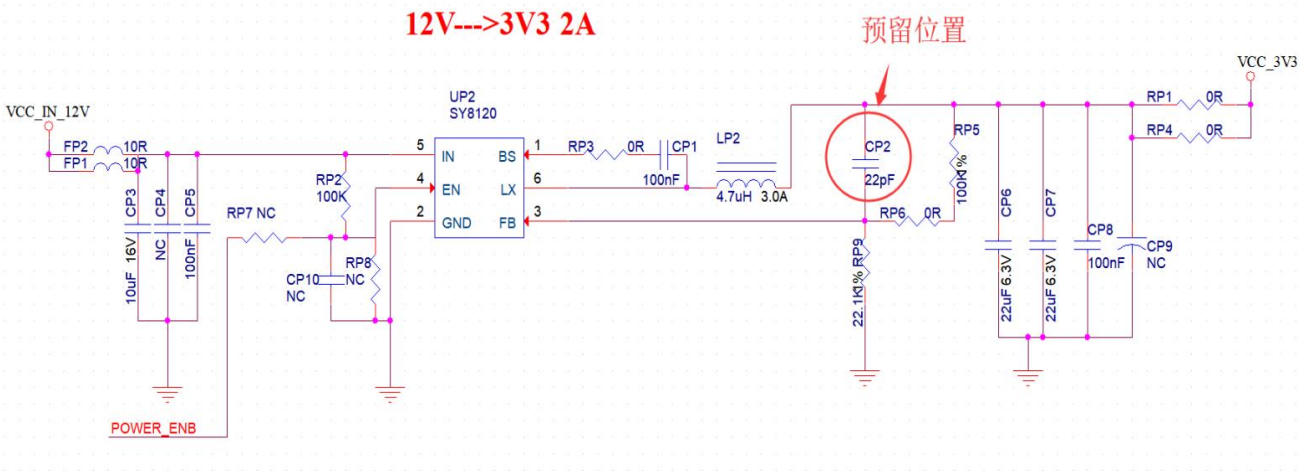


Figure 12 DC-DC buck circuit diagram

6.7. GPIO

- Some IO ports are drawn from the periphery of the module. If necessary, it is recommended to use 10-100 ohms in series resistance on the IO port. This suppresses overshoot and makes both sides smoother. Helps with both EMI and ESD.
- To pull up and down special I/O ports, refer to the usage instructions in the specifications. This affects the startup configuration of the module.
- The I/O port of the module is 3.3V. If the level of the master control does not match that of the I/O port of the module, a level conversion circuit needs to be added.
- If the I/O port is directly connected to the peripheral interface or a pin bar terminal, reserve an ESD device near the I/O port cable to the terminal.

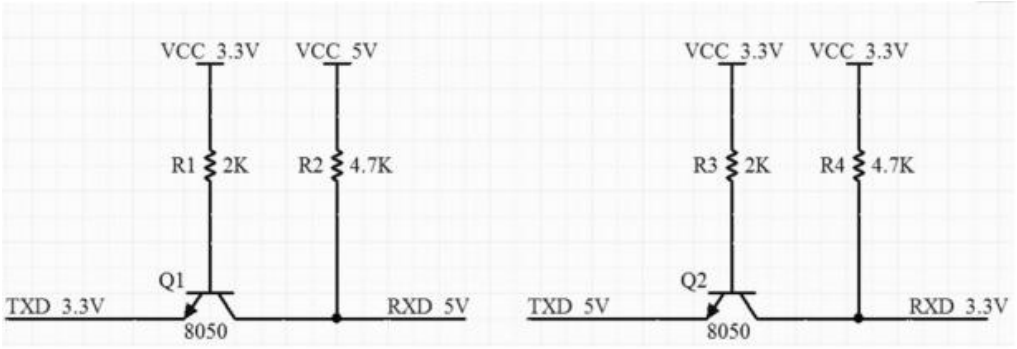


Figure 13 Level switching circuit

7. Storage conditions

Products sealed in moisture-proof bags should be stored in a non-condensing atmospheric environment of <40 ° C /90%RH.

The module has a moisture sensitivity level MSL of level 3.
After the vacuum bag is unsealed, it must be used within 168 hours at 25±5℃/60%RH, otherwise it needs to be baked before it can be put on line again.

8. Flow welding curve diagram

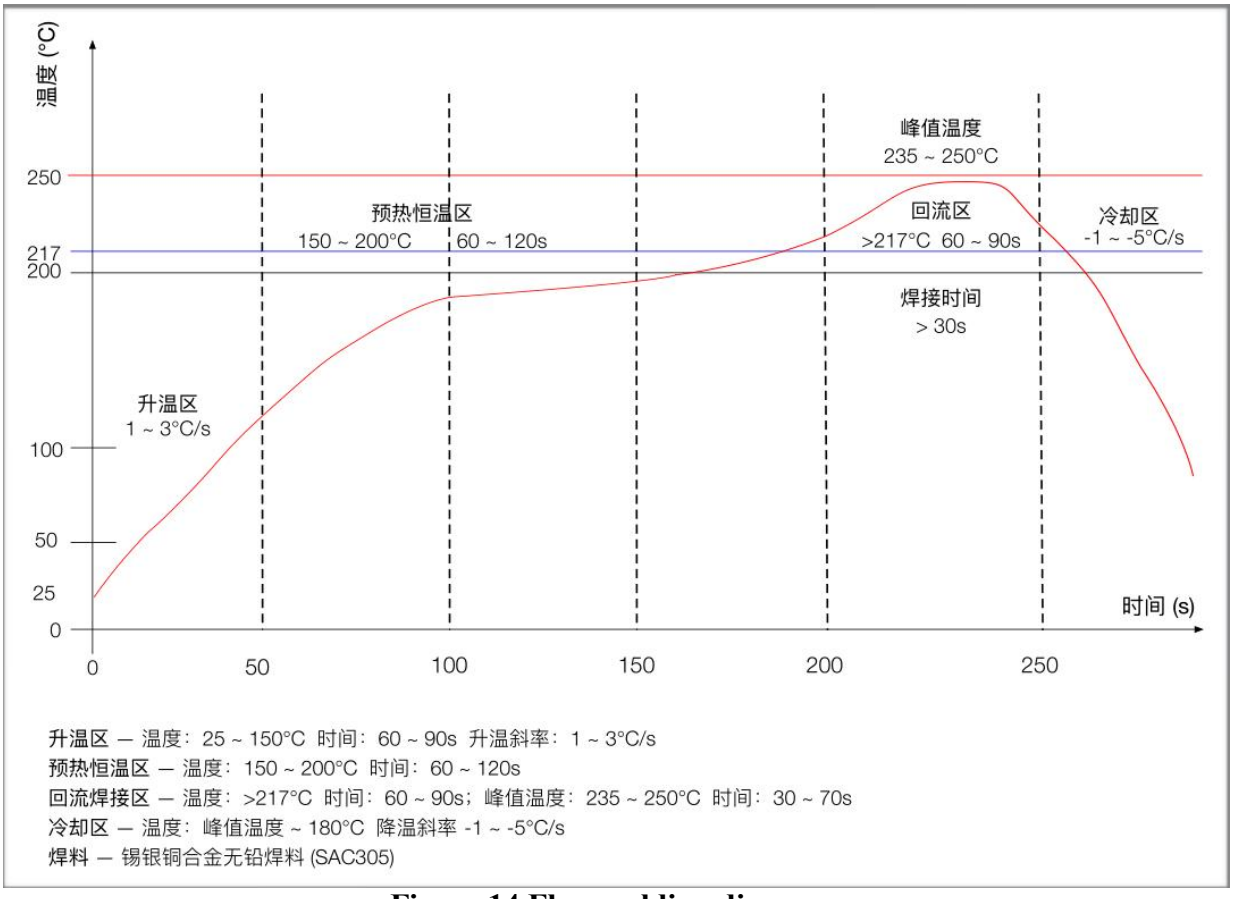


Figure 14 Flow welding diagram

9. Product packaging information

BU03 module adopts braid packaging, 950pcs/ disk. As shown in the picture below:

Figure 15 Package and packing diagram

10.Contact us

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